Guest lecture on "Processor and memory Technology"

DATE: 5/4/2021

Event Coordinator(s)

1. Prof. Tejal Deshpande

Student Coordinator(s)

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Time & Place:

5th April,2021

11am to 1pm

Platform: Online (Google Meet)

Department:

EXTC

No of participants:

100

Mr. Atul Oak, Assistant Professor, Vidyalankar Institute of Tecnology, Wadala delivered a Guest lecture on **"Processor and Memory Technology"** on Monday 5th April, 2021 for Second Year & Third Year students of the Department of Electronics & Telecommunication.

Because of COVID-19 pandemic situation the guest lecture was conducted on Google Meet online platform.

100 participants from S.E & T.E attended the session. Some of the important topics covered were Pipelined, Non pipelined, Hybrid architecture, Cache Memory,Paging etc

The participants found it very informative and well organized. They look forward for more sessions on Memory Management

Signing Authority Name and Designation	Signing Authority Name and Designation	Signing Authority Name and Designation

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eedback from Participants:

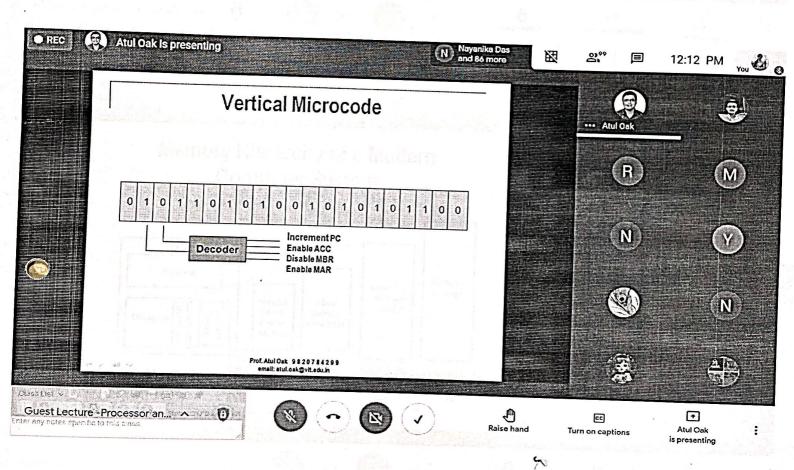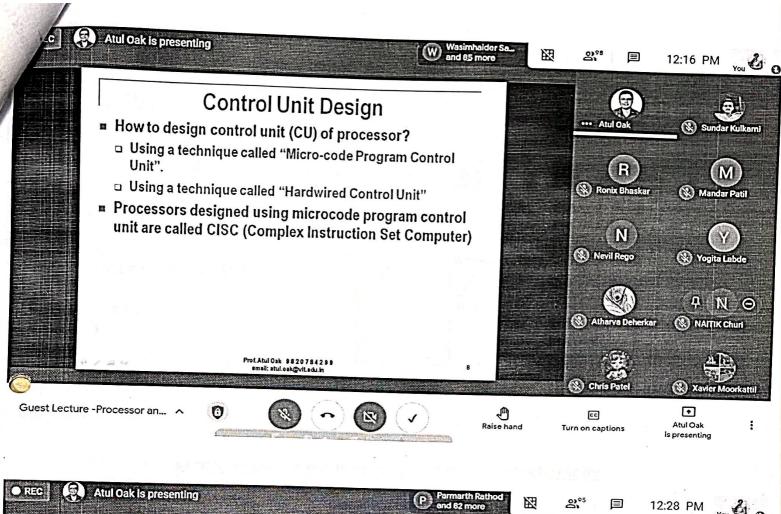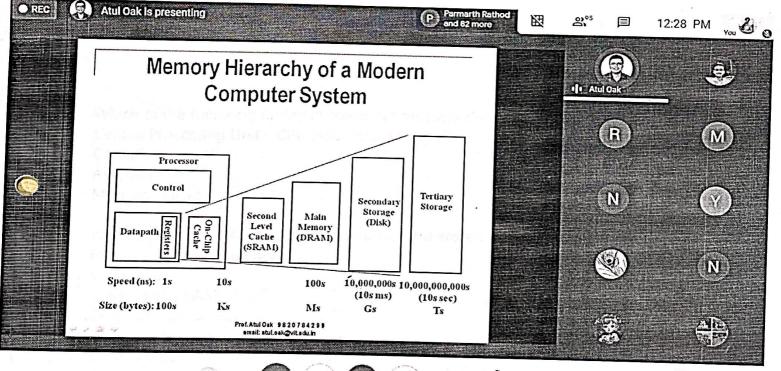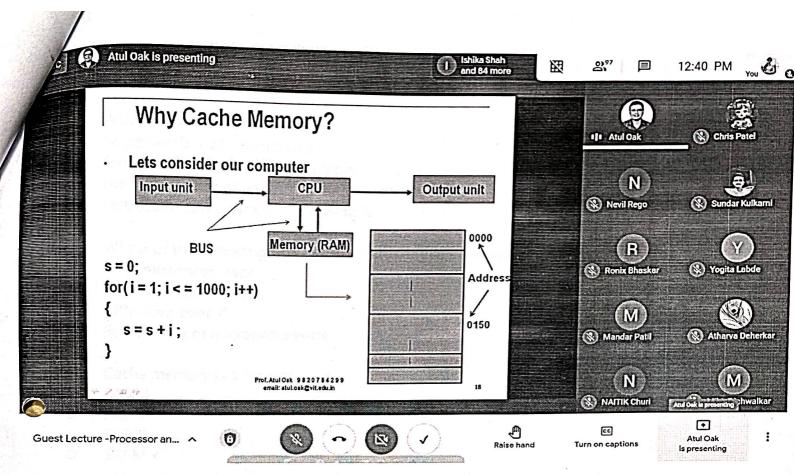| |
|---|
| The session was great and interesting. |
| It was helpful learnt something new |
| Very helpful. Thank you. |
| great level of communication. Thank you |
| Session was great 👍 |
| Very Interesting and Awesome session. |
| interesting session |
| Lecture was interesting but want to know more about this topic |
| More sessions on Quantum Computing |
| Good session |
| Informative |

Control Unit Design

- How to design control unit (CU) of processor?
  - Using a technique called "Micro-code Program Control Unit".
  - Using a technique called "Hardwired Control Unit"
- Processors designed using microcode program control unit are called CISC (Complex Instruction Set Computer)

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Memory Hierarchy of a Modern Computer System

	Processor				
	Control				
	Datapath / Registers	On-Chip Cache	Second Level Cache (SRAM)	Main Memory (DRAM)	Secondary Storage (Disk)	Tertiary Storage

Speed (ns):   1s   10s   100s   10,000,000s   10,000,000,000s
                                              (10s ms)   (10s sec)
Size (bytes): 100s   Ks   Ms   Gs   Ts

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Why Cache Memory?

- Lets consider our computer

Input unit → CPU → Output unit

BUS   Memory (RAM)

```
s = 0;
for( i = 1; i < = 1000; i++)
{
    s = s + i;
}
```

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MCQ's taken on the Processor and memory technology

Answer the following Multiple Choice Questions

1 Which of the following facility in computer executes the program?
   A Central Processing Unit – CPU (Microprocessor) ✓
   B Compiler
   C Assembler
   D Memory (RAM)

2 When program is executed in the computer, it is stored in ___.
   A Memory like disk memory
   B I/O devices
   C Memory like RAM ✓
   D CPU (microprocessor)

3 What is CISC?
   A Computer Instruction Set Computing
   B Computing Instruction Set Computer

C Complex Instruction Set Computer ✓
D Complex Instruction Set Communication

What is a feature of RISC?
A Large number of instructions
B Size of the instructions are variable
C Limited number of instructions ✓
D Instruction can perform complex task

5 Which of the following processor/controller use a technique of RISC design?
A 8086 microprocessor
B 8051 microcontroller
C ARM controller ✓
D 80XX family of microprocessors

6 Cache memory is a type of ___?
A DRAM
B PROM
C EPROM
D SRAM ✓

7 Select the appropriate function of cache memory.
A To bridge speed difference between processor and main memory(RAM) ✓
B To store large data
C To increase complexity of machine
D To store data permanently.

8 Select correct statement about cache memory?
A Cache miss should be ideally 1
B Cache hit should be ideally 1 ✓
C Cache hit should be ideally 0
D Cache miss as large as possible.

9 Which technique is used for the design of CISC processors?
A Hard wired control unit
B State table approach
C Delay element approach
D Microcode program control unit ✓

10 Select the correct sequence the program is executed in the computer.

A   Fetch→Execute→Decode
B   Decode → Fetch → Execute
C   Decode → Execute →Fetch
D   Fetch → Decode → Execute ✓